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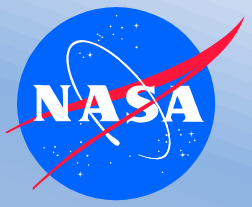

Isolating Memory Arrays in SEE Testing of Commercial Memory Components

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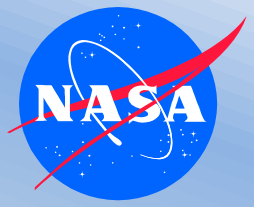

Outline

- Background – the need for space memory
- Memory-array data
- SEE test methods focused on the memory array
- Results & Discussion DDR2
- Results & Discussion MRAM
- Future Work
- Conclusions

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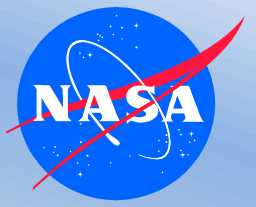
Space Memory Study



- Selection of memory for space mission:
  - Reliability (including radiation)
  - SWaP
  - Application needs
- Study reported last year at RADECS pointed out parameters for needed space memory
  - Errors limited to SBUs, no SEFIs resulting in more than 1 bit error in a single address
  - Need devices with at least 100 krad(Si) survivability
- But all current devices have problems
  - Chip density is too low
  - Cannot provide radiation performance
  - Require too much power

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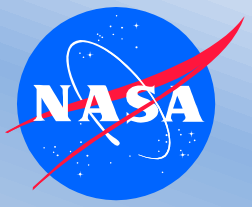


Path to a Device

- We need Rad Hard memories (devices)
- Rad Hard memory arrays exist (we believe)
  - Due to memory cell type and scaling
  - Not intentional
- Commercial devices have controllers with radiation problems.
  - E.g. DDR SEFIs
- A memory development that involves commercial memory mounted to a rad hard controller needs radiation data.

Why Memory Arrays?

- Example: DDR2
  - We have been working on a DDR2 device that had a recent revision
    - The earlier device has 50x lower SEFI rate than the new device
    - But the new device has lower bit-level SEEs
- Memory arrays? Why not memory cells?
  - The cells don't live in a vacuum, they have to be made in macros with 1e3-1e5 or more bits. Macros are repeated 100s-1000s of times (or more) to make a device.
  - Support circuitry of some type must be present
    - At least local selectors
    - DDR2 has local sense-amplifiers

Commercial Arrays

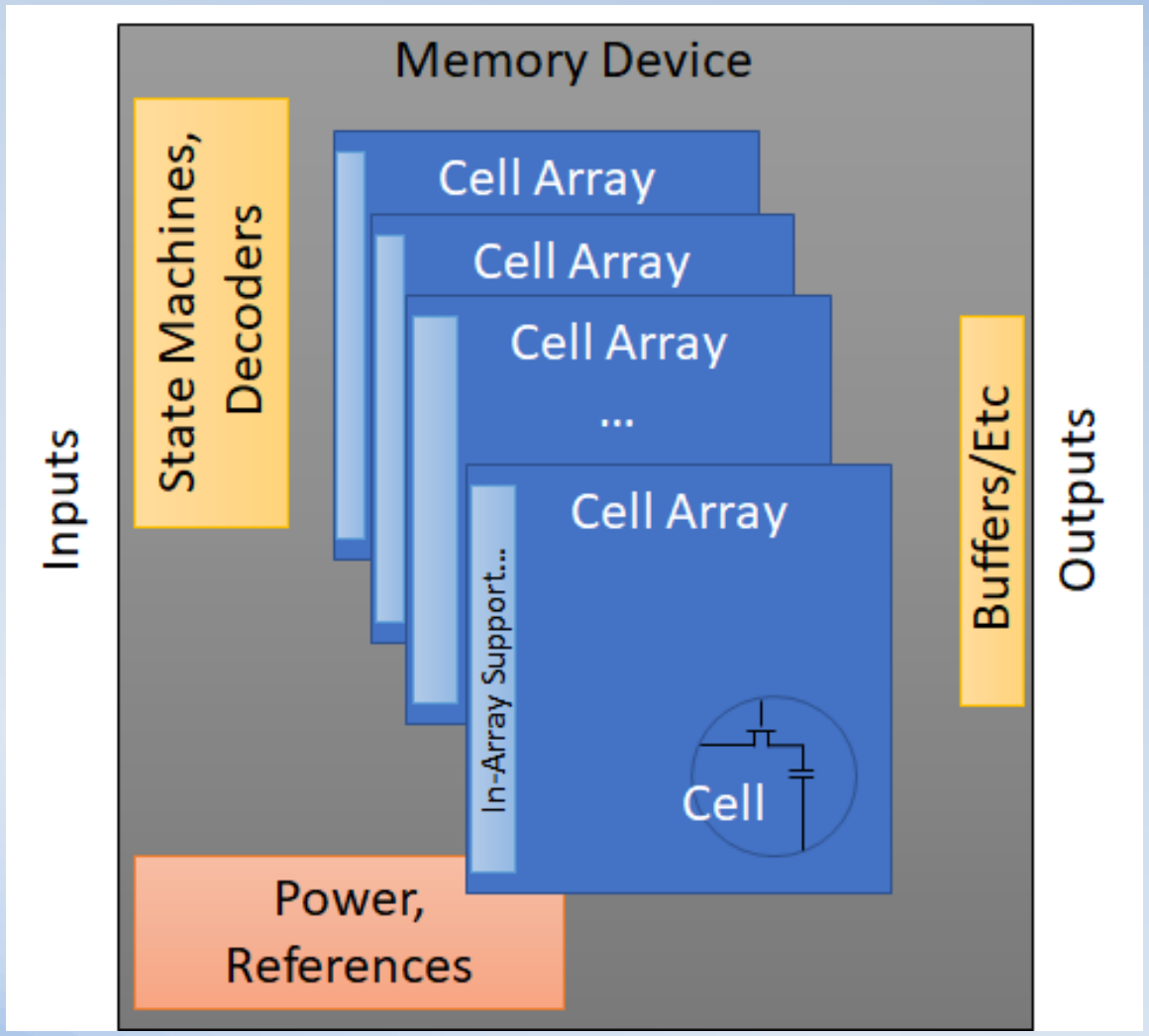
- We spoke with several manufacturers about obtaining test arrays.
- The expedient approach, for them, was to inform us of commercial devices that contain their memory arrays.
- Rather than evaluating test structures, we had the option of testing the arrays in the commercial devices (and we could test immediately).
  - Also helps with being able to evaluate more technologies with fewer partnering issues short-term
- But then the question becomes: how do you isolate the radiation performance of the array.
  - For cells, this is straightforward
  - For SEFIs, it is unclear…

Are All SEFIs Bad?

- From this type of test, there are two sources of SEFI
  - Those in the control logic that can be removed from the device and replaced – problem solved!
  - Those in the control logic that cannot be removed

- In fact, almost all SEFIs are not bad.
  - What we really need to know is:
    - How many of them are there? (rate)
    - What is the (rough) structure?
  - Realistically the only “bad” SEFI is one that might lose data in an entire cell-array macro
    - In theory, if the cell arrays are small enough the controller can handle this through redundancy and error correction

Commercial Devices



Cartoon of memory device structure indicating the "cell array", which may be a repeated structure. If the cell array is robust to radiation effects, it should be possible to build the rest of the circuit in RHBD to provide desired performance.

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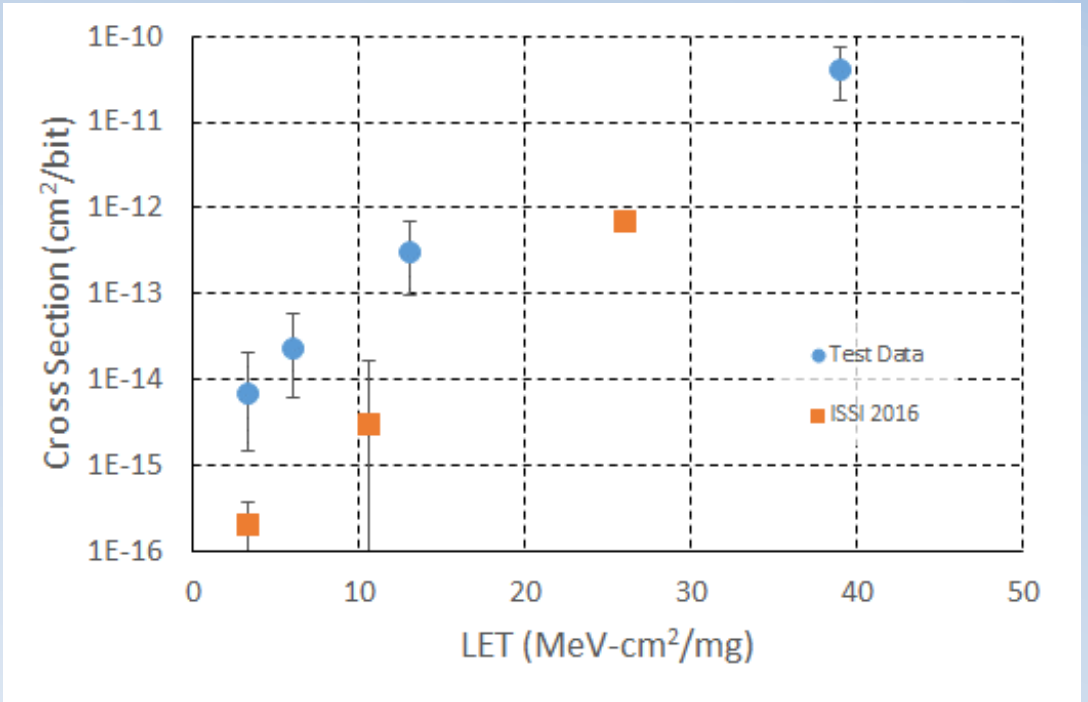
(SEE) Test Approach

- Options
  - Test unbiased – cells only – but only works on non-volatile
  - Test at low speed – eliminate any high-speed interface issues
    - The timing in the cell array is assumed to be independent of the interface timing
  - Determine SBU information, but focus is on SEFIs and damage

- Generally, standard testers (& methods) should also be used, but they may confuse things
  - Industrial reliability testers can verify devices are working correctly
  - These focus on reliability issues and are very helpful for damaging SEE and TID
  - Do not provide the type of stimulus needed for SEE testing, but can provide a double-check of questionable results

DDR2 SBU Sensitivity

- Test device exhibited SBUs
  - No multiple-bit upsets observed in a single address
- Compared to other DDR2 device (ISSI tested in 2016)
  - Note this old ISSI device is an example of rad-hard by luck
    - It is 10-20x lower cross section in the “knee region” than other devices from the same generation.
  - The tested device is consistent with expected SBU performance



Single Bit Upset sensitivity of tested DDR2 device
Compared to ISSI DDR2 used in some missions.

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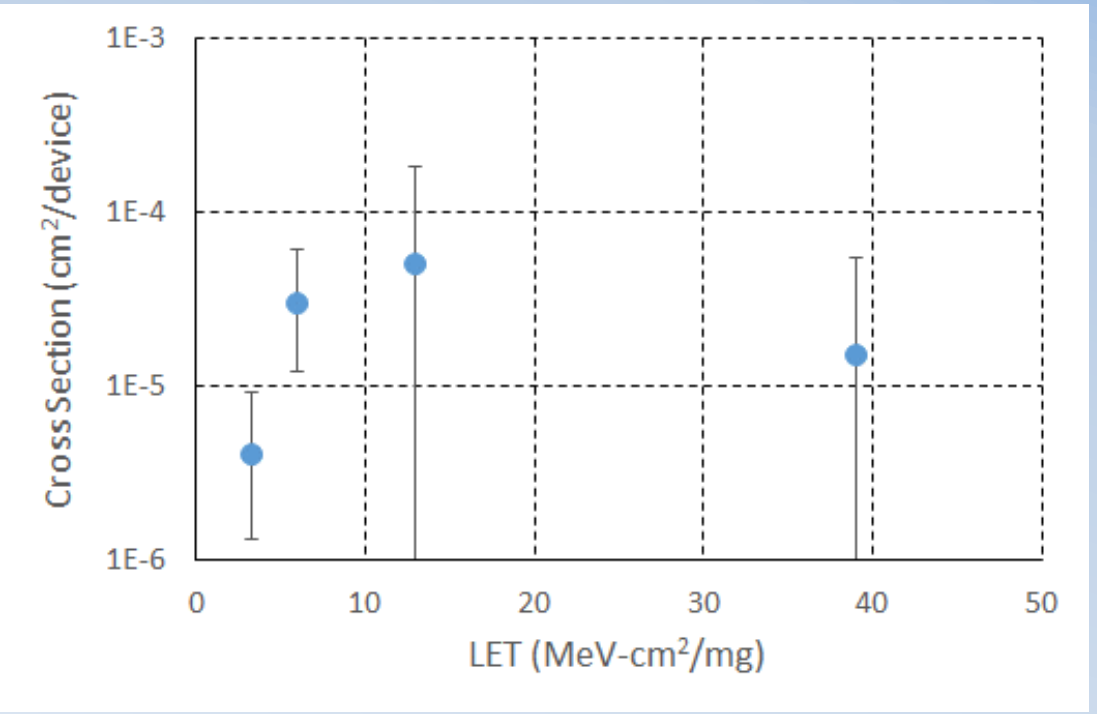
DDR2 SEFI Sensitivity

- No SEL: 1.9V, 95C, using 2×10^7 /cm^2 @ LET 83 MeV-cm^2/mg
- Tested DDR2 devices showed SEFIs
- Two types of SEFIs (rough)
  - Millions of errors
  - Thousands of errors
- Large SEFIs are the result of the controller
- Small SEFIs may be intrinsic to the cell array
  - (Row SEFI, where all bits on a row are lost)



DRAM SEFI sensitivity. Note that many SEFIs resulted in the device showing millions of errors.

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DDR2 Discussion

- Bit errors – essentially a “don’t care” – controller can perform error correction
- Row SEFIs (word line activation)
  - Definitely in the memory array, must be handled by spreading ECC bits to avoid multi-bit errors
- Column SEFIs (any small SEFI that is recovered by reinitializing)
  - Clearly the data is never lost, but the device forgets where to get it and returns bad data to the system
  - This is a controller-level issue that can be handled
- “MSEFI” (device goes “out to lunch”)
  - Clearly this is a device level control failure – all data are lost
  - Can be fixed by rad hard controller
- Read SEFI (rereading works fine)
  - The exact cause of this type of event is believed to be decoding or failure to process a command
  - It is very unlikely that this is at the cell level, because cells that make up a single read are spread throughout the chip. But this error appears as though all bits are read incorrectly.

MRAM SEL, SBU

- No SEL - LET of 84 MeV-cm^2/mg, 1×10^7 /cm^2 exposure

- No SBU – tested in unbiased mode
  - Non-volatile cells could easily be isolated this way

Ion	Energy	LET	Fluence	Bit Errors
Ne	25 Mev/amu	1.9 MeV-cm2/mg	2.00E+07	0
Ar	25	7.6	2.00E+07	0
Kr	25	33.7	2.00E+07	0

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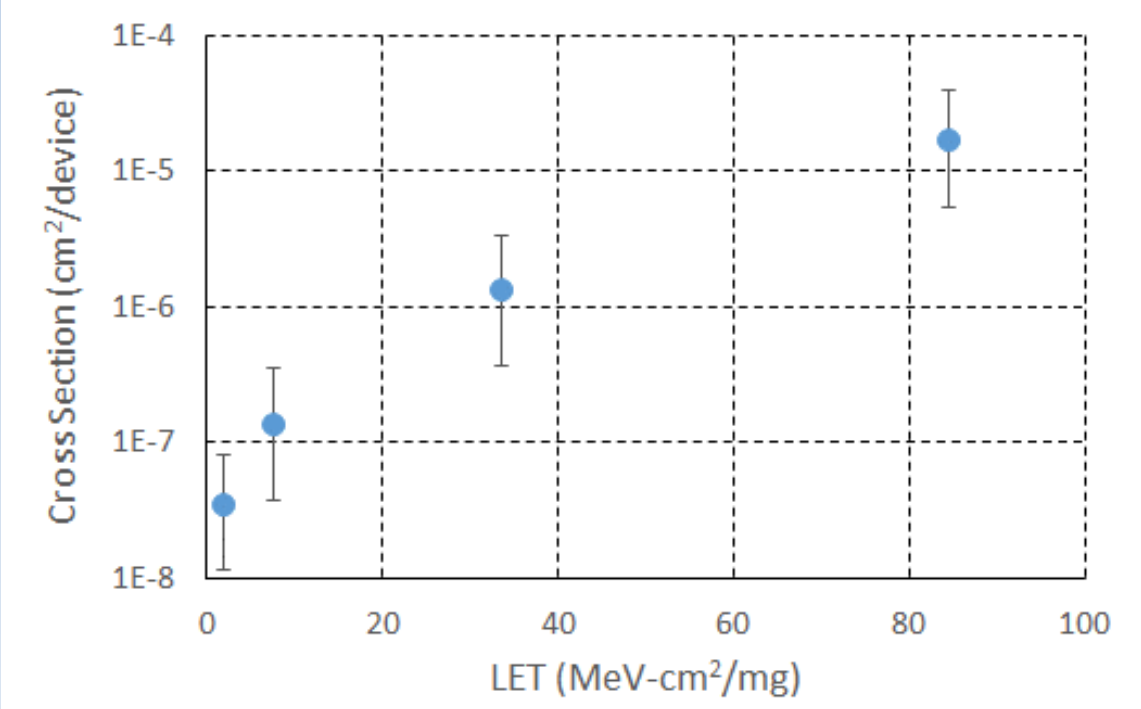
MRAM SEFI

- One interesting behavior observed in the MRAM test devices was a SEFI that resulted in all data being lost.
- This behavior is attributed to the control circuitry and is expected to be possible to mitigate in a production device.



Sensitivity of MRAM to device-wide SEFI

MRAM Discussion

- Bit errors – none observed (we think there is a level that would cause some, but consider them negligible – we saw none with 1e7/cm2 at LET 75 MeV/cm2-mg.
- Device data loss SEFI
  - We can eliminate this at the array level because it is all or none – suggesting a global error
  - It is possible that a local controller could erroneously trigger an erase cycle, but we would expect to see portions of the device go bad. We tested for this and it was not seen.

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Conclusion

- Because of SEFIs and performance requirements, there is no good memory for high reliability space applications.
  - But SEFIs are primarily the result of control circuitry.
  - With adequate understanding of the cell-array, SEFIs can be either eliminated or handled by a rad hard controller mated to the memory.
- We focused on commercial memory arrays
  - Manufacturers proved to be willing to inform us of memory technology available in commercial devices, as opposed to providing test structures.
  - In reality, it is the combination of the cells and cell-array macros that we need.
  - Tests focused on how to isolate memory-array performance aside from overall device-level control structures that can be replaced.
- DDR2 device SEFIs from a tested device proved to be as expected, and our data can be used to evaluate if a proposed memory controller will adequately handle all event types.
- MRAM devices had only one type of event that showed SEE sensitivity – a device-wide permanent loss of data – similarly this can be used as a test case to evaluate a proposed rad-hard controller.